REMARKS/ARGUMENTS

This Response is submitted in reply to the Office Action dated March 1, 2006, and within the three month period for reply extending to June 1, 2006. Claims 1-22 remain pending following entry of this Response.

Rejections under 35 U.S.C. 102

Claims 1, 8, 15, and 21-22 were rejected under 35 U.S.C. 102(b) as being anticipated by Bennett (U.S. Patent No. 5,404,464). These rejections are traversed.

With regard to claim 1, the Office has asserted that Bennett teaches at least one register in communication with a shared resource, wherein the at least one register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal. More specifically, the Office has asserted that the Last Slot ID Register (62) in the Bandwidth Maximizer Circuit (38) of Bennett teaches the at least one register of claim 1. As explained below, the Applicants respectfully disagree with this assertion by the Office.

Bennett (7:43-49) teaches that the Last Slot ID Register (62) is configured to hold, i.e., store, the "Slot ID" of the last address request that was made. Bennett (6:2-7) teaches that the "Slot ID" represents the slot number of a memory module (14). Therefore, Bennett teaches that the "Slot ID" of the last address request is actually the slot number of the memory module (14) that contains the last address that was requested. It should be appreciated that the "Slot ID" as taught by Bennett is not equivalent to an address. This fact is further clarified in the discussion provided by Bennett at (6:50-61), as provided below:

"In the present embodiment, the system memory is divided into blocks of 1 megabyte each. Thus, the slot numbers stored in each location of the slot I.D.

mapping SRAM 60 are assigned on the basis of the 1-megabyte divisions of memory. For example, if the first megabyte of memory is mapped to a memory module 14 in slot 3 and the second megabyte of memory is mapped to a memory module 14 installed in slot 4, the computer operating system stores the identifier "3" (011 in binary) in the first location of the slot I.D. mapping SRAM 60, and the identifier "4" (100 in binary) in the second location of the slot I.D. mapping SRAM 60."

In view of the foregoing, the Applicants submit that the Last Slot ID Register (62), as taught by Bennett, does not in fact teach the register configured to hold an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 1. Additionally, the Applicants do not find another teaching in Bennett that would anticipate the register of claim 1.

Further with regard to claim 1, the Office has asserted that Bennett teaches a multiplexer for providing a next address to the at least one register. More specifically, the Office has asserted that the multiplexer (56) of Bennett teaches the multiplexer of claim 1. However, because Bennett does not teach the at least one register, as noted above, it is not possible for Bennett to teach a multiplexer for providing a next address "to the at least one register."

The foregoing notwithstanding, the multiplexer 56 of Bennett does not teach the feature of claim 1 regarding "the multiplexer being disposed outside of a critical timing path for addressing the shared resource." Figure 4 of Bennett and the associated discussion teach that the multiplexer 56 is connected between the address bus 70 and the early address signal line 84 that communicates with the bus controller 36. The early address signal to be provided to the bus controller 36 cannot be generated until the multiplexer 56 provides input to the Slot I.D. Mapping SRAM 60 so that the Last Slot

I.D. Register 62 can be set. Therefore, it should be appreciated that the multiplexer 56 is in fact within the critical timing path for addressing the shared memory module 14.

The Office has referred to the teachings of Bennett at (6:40-44) as anticipating the feature of claim 1 regarding the multiplexer being disposed outside of a critical timing path for addressing the shared resource. However, beyond simply quoting Bennett (6:40-44) the Office provides no further explanation as to how Bennett (6:40-44) is being interpreted to teach the multiplexer being disposed outside of a critical timing path for addressing the shared resource, as required by claim 1. The teaching of Bennett (6:40-44) does not on its face suggest that the multiplexer 56 is disposed outside of a critical timing path for addressing the memory module 14. Moreover, the teaching of Bennett (6:40-44) indicates that the multiplexer 56 is in fact disposed within the critical timing path for addressing the memory module 14.

In view of the foregoing, the Applicants submit that the multiplexer 56, as taught by Bennett, does not teach the multiplexer as required by claim 1. Additionally, the Applicants do not find another teaching in Bennett that would anticipate the multiplexer of claim 1.

For at least the reasons discussed the Applicants respectfully submit that Bennett fails to teach each and every feature of claim 1. The Office is reminded that a claim is anticipated under 35 U.S.C. 102 only when each and every feature of the claim is taught by a single prior art reference. Because Bennett does not teach each and every feature of claim 1, as discussed above, Bennett does not anticipate claim 1 under 35 U.S.C. 102. Therefore, the Office is kindly requested to withdraw the rejection of claim 1. Also, because each of dependent claims 2-7 incorporates all the features of claim 1, the Applicants submit that each of claims 2-7 is patentable for at least the same reasons provided for claim 1.

With regard to claim 8, the Office has asserted that Bennett teaches at least one register configured to provide an address to an address port of a shared memory upon receipt of a clock signal. More specifically, the Office has asserted that claim 5 of Bennett (17:5-19) teaches the register of claim 8. The static random access memory recited in claim 5 of Bennett corresponds to the Slot I.D. Mapping SRAM 60 in the Bandwidth Maximizer Circuit (38) of Bennett. Also, the storage register recited in claim 5 of Bennett corresponds to the Last Slot I.D. Register 62 in the Bandwidth Maximizer Circuit (38) of Bennett. Therefore, the arguments presented above with respect to the at least one register in communication with a shared resource as recited in claim 1 are equally applicable to the at least one register recited in claim 8.

Additionally, the Office has referred to the teachings of Bennett at (6:40-44) as anticipating the feature of claim 8 regarding the multiplexer being disposed outside of a critical timing path for addressing the shared memory. Therefore, the arguments presented above with respect to the multiplexer recited in claim 1 are equally applicable to the multiplexer recited in claim 8.

For at least the reasons identified above, the Applicants respectfully submit that Bennett fails to teach each and every feature of claim 8. Therefore, Bennett does not anticipate claim 8 under 35 U.S.C. 102. Thus, the Office is kindly requested to withdraw the rejection of claim 8. Also, because each of dependent claims 9-14 incorporates all the features of claim 8, the Applicants submit that each of claims 9-14 is patentable for at least the same reasons provided for claim 8.

With regard to claim 15, the Office has asserted that Bennett (8:13-28) teaches loading at least one register with an address to be provided to the shared resource, and providing the address to the shared resource from the at least one register upon receipt of a clock signal. Once again, the Office has referred to the Last Slot I.D. Register 62 in the

Bandwidth Maximizer Circuit (38) of Bennett as teaching the register loaded with an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 15. As previously discussed with respect to claim 1, the Last Slot ID Register (62) of Bennett is configured to store a "Slot ID" of the last address request that was made, wherein the "Slot ID" represents the slot number of a memory module (14). It should be appreciated that the "Slot ID" is not an address to be provided to a shared resource, i.e., to a shared memory. Therefore, the arguments presented above with respect to the at least one register in communication with a shared resource as recited in claim 1 are equally applicable to claim 15.

For at least the reasons identified above, the Applicants respectfully submit that Bennett fails to teach each and every feature of claim 15. Therefore, Bennett does not anticipate claim 15 under 35 U.S.C. 102. Thus, the Office is kindly requested to withdraw the rejection of claim 15. Also, because each of dependent claims 16-22 incorporates all the features of claim 15, the Applicants submit that each of claims 16-22 is patentable for at least the same reasons provided for claim 15.

The Applicants submit that claims 1-22 are in condition for allowance and kindly request the Office to issue a Notice of Allowance. If the Examiner has any questions concerning the present Response, the Examiner is kindly requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Response, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP234). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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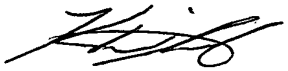

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